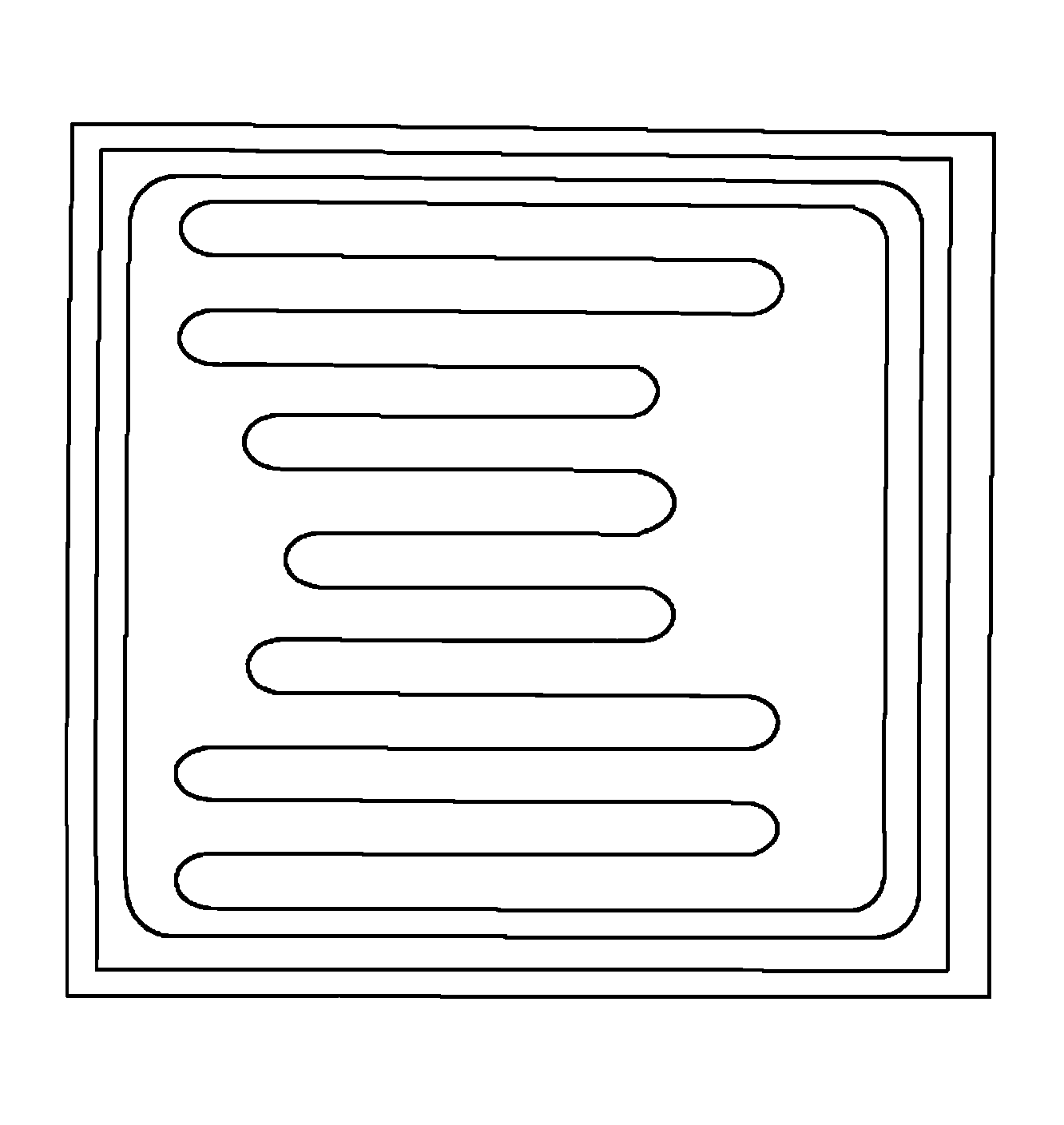
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BASE**

**EMITTER**

**BACK SIDE IS COLLECTOR**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” min.**

**Backside Potential: Collector**

**Mask Ref: AD07**

**APPROVED BY: DK DIE SIZE .097” X .097” DATE: 3/25/16**

**MFG: ON SEMI THICKNESS .013” P/N: MJEC15028 / 15029**

**DG 10.1.2**

#### Rev B, 7/19/02